

# A 200 $\mu\text{m}$ x 200 $\mu\text{m}$ x 100 $\mu\text{m}$ , 63nW, 2.4GHz Injectable Fully-Monolithic Wireless Bio-Sensing System

S. O'Driscoll<sup>#1</sup>, S. Korhummel<sup>#</sup>, P. Cong<sup>#</sup>, Y. Zou<sup>#</sup>, K. Sankaragomathi<sup>#</sup>, J. Zhu<sup>\*</sup>, T. Deyle<sup>^</sup>,  
A. Dastgheib<sup>#</sup>, B. Lu<sup>#</sup>, M. Tierney<sup>#</sup>, J. Shao<sup>#</sup>, C. Gutierrez<sup>#</sup>, S. Jones<sup>#</sup>, H. Yao<sup>#</sup>

<sup>#</sup>Verily (Google) Life Sciences, <sup>\*</sup>Google <sup>^</sup>Cobalt Robotics

<sup>1</sup>stiofani@gmail.com

**Abstract**— A wireless system-on-chip with integrated antenna, power harvesting and biosensors is presented that is small enough, 200 $\mu\text{m}$  x 200 $\mu\text{m}$  x 100 $\mu\text{m}$ , to allow painless injection. Small device size is enabled by: a 13 $\mu\text{m}$  x 20 $\mu\text{m}$  1nA current reference; optical clock recovery; low voltage inverting dc-dc to enable use of higher quantum efficiency diodes; on-chip resonant 2.4GHz antenna; and array scanning reader. In-vivo power and data transfer is demonstrated and linear glucose concentration recordings reported.

**Index Terms**—implant, biomedical, 2.4GHz, antenna array, on-chip antenna, wireless power, backscatter modulation, near field, near field array, optical, electrochemical.

## I. INTRODUCTION

A fully-monolithic injectable 2.4GHz wireless sensing SoC is presented - so small that it can be injected painlessly in the skin,  $\leq 250\mu\text{m}$  on each side [1], and is not visible once injected thus enabling truly unobtrusive ongoing monitoring. The skin is a vital organ from which many health metrics may be garnered. For example skin hydration and body glucose levels have been monitored using needles in the skin but those needles can cause discomfort and impinge on users' lifestyle. This paper describes innovative circuit designs required to achieve the small size and monolithic integration; presents an in-vivo power and data transfer demonstration; and highlights an electrochemical (e.g. glucose) sensing instantiation. Fig 1 shows a block diagram of the SoC. The top panel illustrates the scheme to harvest clock and power from an amplitude modulated optical signal transmitted by a reader which is placed on the surface of the skin. Five 44 $\mu\text{m}$  x 44 $\mu\text{m}$  on-chip diodes are used for the main supply and two each for the clock recovery supply and clock input. The grey dashed boxes show different sensor interface schemes (electrochemical, light and capacitive). The reader transmits an RF signal and each sensor interface generates a digital modulation signal for the backscatter-based data uplink.

## II. OPTICAL LINK

Quantum efficiencies (QE) of four diode test structures, Fig 2(a), are plotted in the first panel of Fig 2(b). Psub-to-Nwell (D3) diodes were most efficient irrespective of

wavelength and so were chosen for photovoltaic harvesting. The data shows higher QE at visible wavelengths than in near-IR. Optical transmission versus wavelength was evaluated for numerous porcine skin samples. Results for two representative samples, second panel of Fig 2(b), show better transmission in near-IR consistent with [2]. This indicates a skin-transmission vs diode quantum efficiency tradeoff. Furthermore the maximum permissible exposure (MPE) [ANSI Z136.1], shown in the third panel of Fig 2(b), is not constant versus wavelength. The fourth panel of Fig 2(b) is the calculated available electrical power, based on the three plots above, and shows that 900nm results in the maximum power on-chip.

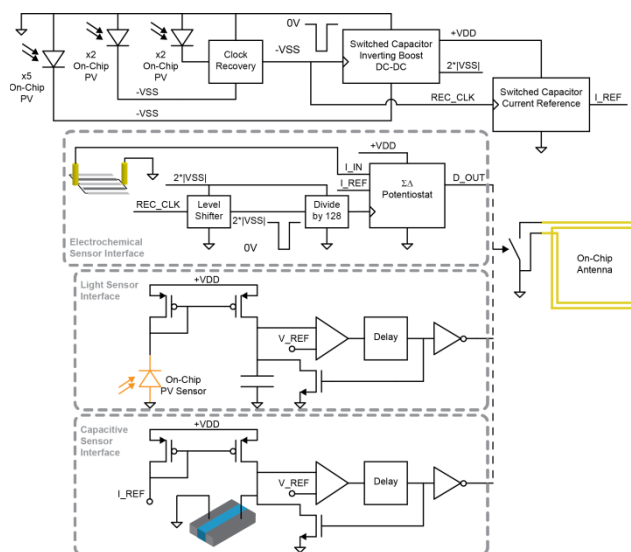


Fig. 1. Block Diagram of Monolithic Injectable Bio-Sensing System. Dashed boxes show electrochemical, light and capacitive sensor interfaces implemented on different instantiations of the SoC.

While the Psub-to-nwell diodes generate greater available power, they unfortunately generate lower open circuit voltage. For the input light energy the voltage generated is -0.3V (relative to Psub, chip ground). The DC-DC converter, Fig 2(c), generates +1.0V from -0.3V. A 3x clock-boosting circuit generates a clock swinging from +0.3V to -0.6V to drive the charge pump switches.

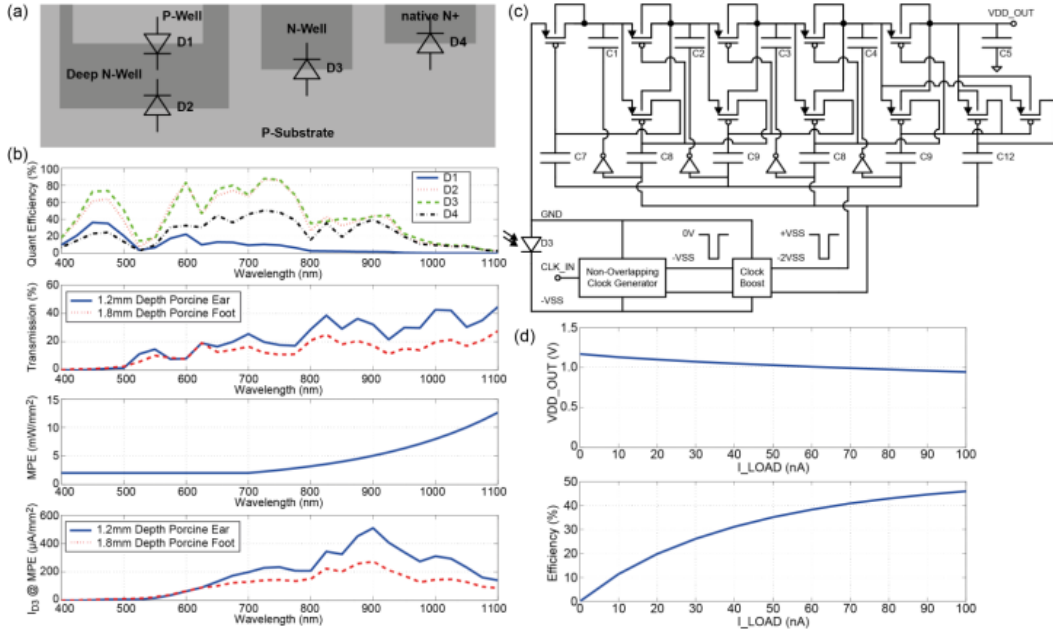


Fig. 2. (a) Candidate photodiodes (b) Measured quantum efficiency of diodes, tissue transmission, maximum permissible exposure and available current vs wavelength (c) -0.3V to 1V charge pump schematic and (d) Measured charge pump output voltage and efficiency vs load current for -0.3V input voltage and 0.9MHz input clock frequency

All NMOS in the clock booster sit in deep Nwells connected to ground. Switches in the charge pump stages are realized using PMOS (deep Nwell NMOS switches are avoided to save area) and are bootstrapped using voltages from successive stages, Fig 2(c). A top metal optical shield reduces leakage in the parasitic photodiodes. The input capacitances are 110fF per stage and the output capacitances are 1.9pF per stage. The entire circuit occupies  $88\mu\text{m} \times 88\mu\text{m}$ .

Fig 2(d) shows the measured output voltage and efficiency versus load current for the charge pump driven by a -0.3V supply with a 0.9MHz clock input. The charge pump efficiency at 100nA load is 46%. The  $200\mu\text{m}$  SoC was demonstrated at 1.3mm depth in porcine skin powered by a 650nm,  $1.9\text{mW}/\text{mm}^2$  source. This demonstrated functionality but not maximum range since 900nm is the optimum wavelength. A  $400\mu\text{m}$  variant of the SoC, accommodating seven times as many PV diodes, was demonstrated at 2.0mm depth in porcine skin powered by a 900nm,  $0.3\text{mW}/\text{mm}^2$  source. We expect a modulate-able MPE-level,  $4.0\text{mW}/\text{mm}^2$  at 900nm, would allow even greater range for the  $200\mu\text{m}$  SoC than the 1.3mm range demonstrated at 650nm.

### III. CLOCK AND CURRENT REFERENCES

A stable on-chip current reference is essential for sensing and current control. A conventional supply independent 1nA reference would require  $92\mu\text{m} \times 92\mu\text{m}$  for the resistor alone, or one quarter of the total SoC area. Instead a switched capacitor current reference was

developed, Fig 3(b), [3]. Transistors M5-M8 form a conventional reference but a switched capacitor circuit formed by M9, M10 and C1 replaces the resistor. C1 is chosen as 20fF to minimize area whilst ensuring the capacitance is large with respect to non-linear variations in the switch input capacitance. Startup branch M1-M4 consumes 15nA at startup and  $< 1\text{pA}$  after startup (worst case). Pseudoresistor M13 and capacitor C3 form a low pass filter to suppress ripple from the switched capacitor. The simulated output ripple is less than 0.15% across corners as the supply voltage varies from 0.4V to 1V. The area of the total circuit is  $13\mu\text{m} \times 20\mu\text{m}$ , 32 times less than would be required for a conventional physical resistor. Fig 3(c) shows a plot of measured output current versus input clock frequency. The target current of 1nA is achieved at the system clock frequency of 0.8MHz and the current can be linearly tuned over more than two decades by varying the clock frequency.

A crystal reference for clock generation would be many times larger than the device. Furthermore the current reference requires a clock input, so clock generation cannot depend on a current reference. Instead the light transmitted to power the chip is amplitude modulated by the reader and that modulation signal is recovered on-chip to generate the clock, Fig 3(a). Two  $44\mu\text{m} \times 44\mu\text{m}$  Psubto-Nwell diodes, D1, are used to generate the supply voltage for the clock recovery circuit, -0.3V to -0.4V. The modulated signal is recovered from identical diode D2, high pass filtered by R1 and C2 and amplified by the inverters. The first inverter could be self-biased using a pseudoresistor and contribute gain but, even with metal

light shielding, photogeneration in the pseudo-resistor would saturate the inverter. Instead unity-gain feedback sacrifices first stage gain but establishes bias for subsequent stages. Metal shielding layers above the circuit are employed to reduce photo-induced inverter offset. All NMOS are deep Nwell with bulk tied to  $-V_{SS}$ . The circuit (excl. D1,2) occupies  $33\mu\text{m} \times 33\mu\text{m}$ , consumes  $45\text{nA}$  and recovers clocks from  $0.1\text{MHz}$  to  $2\text{MHz}$ .

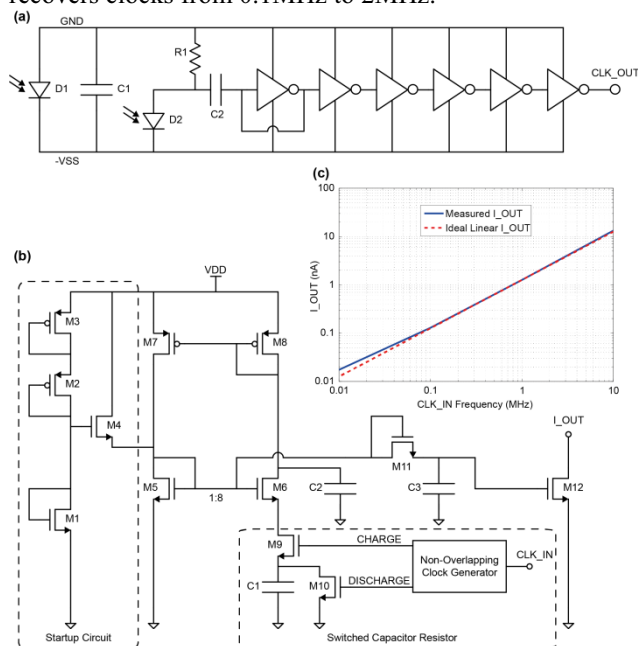


Fig. 3. (a) Clock Recovery Circuit and (b) Switched Capacitor Current Reference Schematic and (c) Plot of Measured Switched Capacitor Reference Output Current versus Input Frequency.

#### IV. WIRELESS LINK: ON-CHIP ANTENNA AND ARRAY READER

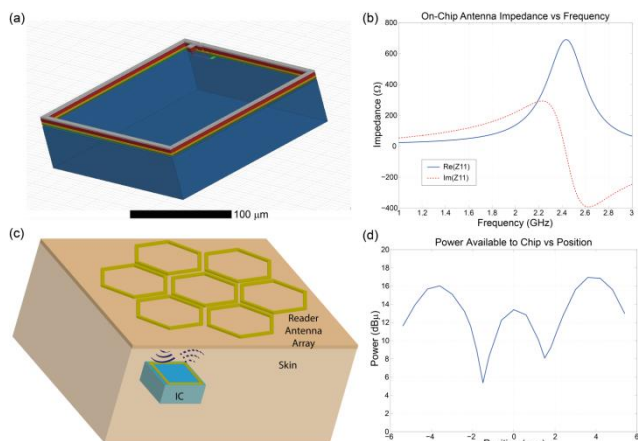


Fig.4. (a) On-chip antenna (b) Simulated on-chip antenna impedance vs frequency (c) Reader antenna array (d) Measured received RF power vs position moving along diameter of array

$2.4\text{GHz}$  is chosen as the operating frequency for the RF link since the receive antenna is sub-mm sized, small

compared to the range and embedded in lossy tissue [4]. Fig 4(a) illustrates the on-chip antenna, multiple turns over many metal layers give an electrically long structure close to self-resonance thus saving area of matching components. A  $25\mu\text{m} \times 10\mu\text{m}$  MIM capacitor provides fine tuning to give antenna impedance shown in Fig 4(b). The reader antenna must not be large compared to the  $200\mu\text{m}$  SoC antenna in order to maximize link gain, making alignment difficult. A scanning antenna array at the reader, in Fig 4(c), makes alignment easier. Optical power and data is transmitted through holes in the middle of each array element. The measured RF power received for a test chip which a rectifier across the antenna at  $1.4\text{mm}$  depth in galline skin, Fig 4(d), shows RF data link viability across the array.

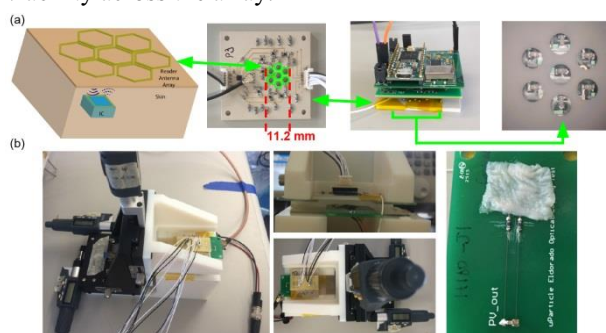


Fig.5. (a) Reader array board, (b) Dual axis alignment test fixture

The current prototype reader comprises a stack of four PCBs and occupies an area of  $18\text{cm}^2$ . The reader array board, Fig.5 (a), is made using a high dielectric Rogers material and an array of LEDs on the bottom side of the board above provide light power through the center of the antenna array elements and are modulated to transmit clock to the injectable SoC. The scanning array and impedance tuning is implemented on board and all is controlled by a microcontroller. Fig. 5(a) from left to right illustrates conceptual reader antenna array communicating with implant; realized 7-element antenna array; full stack reader; bottom view of full stack reader showing near-IR LEDs visible through holes in antenna array elements. Fig 5(b) illustrates the dual axis alignment fixtures which were used together with a pinned out test SoC on a PCB to measure alignment and range ex-vivo (this is the source of the data in figure 4(d)).

#### V. COMPLETE SENSING SYSTEM

The electrochemical sensing system was first implemented on a larger die to accommodate bond pads, that die was affixed to a  $1.5\text{mm} \times 0.7\text{mm}$  glass slide on which a  $200\mu\text{m} \times 200\mu\text{m}$  electrochemical sensor had been patterned and functionalized and the potentiostat input was wirebonded to the sensor, Fig 6(a), to demonstrate system functionality and the feasibility of glucose measurement with such a small sensor. We also have devices with



through silicon vias to allow fabrication of sensors on the backside, Fig 6(b). The glass slide device was placed in controlled concentrations of glucose in saline solution and powered by the reader. The potentiostat is a  $\Sigma\Delta$  ADC [5] and the digital output modulates the backscatter link. The reader demodulated the ADC output which is plotted vs glucose concentration, Fig 6(c), and shows good linearity.

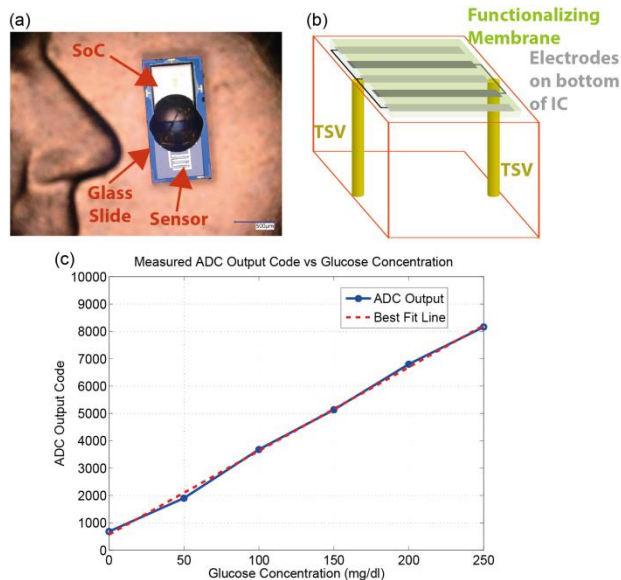


Fig. 6. (a) Test chip with  $\Sigma\Delta$  potentiostat wire bonded to  $200\mu\text{m} \times 200\mu\text{m}$  electrochemical sensor (b) Illustration of planned monolithic glucose sensor with electrode patterned on bottom side of IC and connecting to circuitry through TSVs (c) Measured ADC output from glass slide device in controlled glucose concentration flow cell recorded over the air.

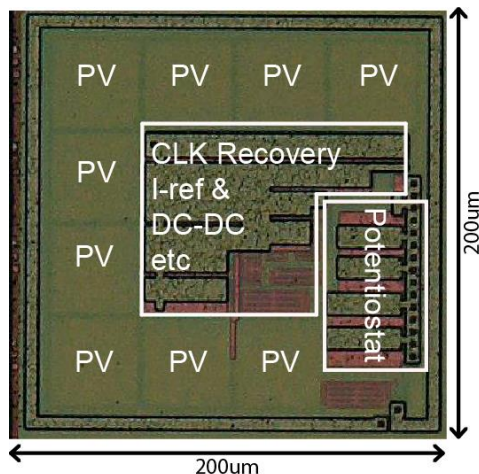


Fig.7. Die Photo: The antenna top layer is visible as the  $5\mu\text{m}$  wide,  $200\mu\text{m} \times 200\mu\text{m}$  square around the perimeter. Nine squares corresponding to the nine  $44\mu\text{m} \times 44\mu\text{m}$  diodes used for photovoltaic harvesting of clock and power are visible along the top, left and bottom side. The metal visible above the other circuits is for light shielding.

TABLE I  
PERFORMANCE SUMMARY

IC Technology	65nm CMOS
Device Size	$200\mu\text{m} \times 200\mu\text{m} \times 100\mu\text{m}$
Photovoltaic Area	$135\mu\text{m} \times 135\mu\text{m}$
Circuitry Area	$125\mu\text{m} \times 125\mu\text{m}$
Optical Wavelength	900nm
Chip Power consumption	63nW
Demonstrated Range in Porcine Skin Model	1.3mm for $200\mu\text{m}$ SoC @ $\lambda=650\text{nm}$ (RED) @ $1.9\text{mW}/\text{mm}^2$ 2.0mm for $400\mu\text{m}$ SoC @ $\lambda=900\text{nm}$ (Near-IR) @ $0.3\text{mW}/\text{mm}^2$
Antenna Loop Area	$200\mu\text{m} \times 200\mu\text{m}$
Alignment Window	11.2mm diameter circle
<b>Clock Recovery</b>	
Area	$33\mu\text{m} \times 33\mu\text{m}$
Operating Range	0.1MHz to 2MHz
Power Consumption	16 nW
<b>Current Reference</b>	
Area	$13\mu\text{m} \times 20\mu\text{m}$
Output Current	1nA
Linear Tuning Range	0.12nA to 11nA
Supply Sensitivity ( $I_{\text{out}}/V_{\text{DD}}$ )	50pA/100mV
Ripple (simulated)	< 0.15% across corners
Power Consumption @ 1nA output	7.4 nW
<b>-0.3V to +1.0V DC-DC Converter</b>	
Area	$88\mu\text{m} \times 88\mu\text{m}$
Efficiency (0.9MHz CLK, 100nA load)	46%

## VI. CONCLUSIONS

This paper presents techniques to realize a monolithic wireless system-on-chip small enough to allow painless injection. In-vivo functionality in a leporine model has been demonstrated and ex-vivo sensor recording is reported. The on-chip 2.4GHz antenna and array scanning reader and innovative RF-SoC are key to achieving this small size and functionality.

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